REMARKS

Status Summary

With this amendment, claims 1 and 3 are pending in the present application. Both claims 1 and 3 have been amended. Also Figure 8 has been added and the specification has been amended as discussed above.

Support for Figure 8 and the amendments to the claims and specification can be found through the original specification. For example, in the original claims, at page 3, lines 1-4, page 14, lines 20-35, page 15, lines 12-37, and page 16, lines 36-39.

Drawings

Applicant respectfully submits that the Examiner's objections to the Drawings have been addressed with the addition of Figure 8 and the corresponding amendments to the specification outlined above.

Claim Objections

Regarding the claim objections, applicant has amended the claims to address the examiner's concerns regarding informalities in the claims.

Claim Rejection - 35 U.S.C. § 103

Claims 1 and 3 stand rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,870,620 to Kadosumi, hereinafter referred to as "Kadosumi", in view of Intel's "IA-64 Application Developer's Architecture

Guide," 1999, hereinafter referred to as "Intel Guide." This rejection is respectfully traversed in view of the above amendments and the below remarks.

Claim 1 recites a method for processing conditional jump instructions in a processor with pipeline computer architecture. Claim 1 has been amended to recite loading and decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, which comprises at least one precondition bit that specifies under which conditions the instruction is actually to be executed, and a post-condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Further, Claim 1 has been amended to recite that the post-condition comprises at least one post-condition bit that is checked in the processor. Claim 1 has also been amended to recite checking the precondition, and executing the decoded processor instruction if the precondition is fulfilled. Claim 1 recites that, in the case of a fulfilled precondition, checking the post-condition, and carrying out no jump if the post-condition is not fulfilled, and checking the corresponding flag bits, if the post-condition is fulfilled. Further, Claim 1 recites jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set.

Claim 3 recites an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture. Further, Claim 3 has been amended to recite an instruction decoder operable to decode a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a

precondition comprising at least one precondition bit configured to specify under which conditions the instruction is actually executed, and a post-condition configured to specify a conditional jump is processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Claim 3 has also been amended to recite that the post-condition comprises at least one post-condition bit that is checked in the processor, and the precondition comprises at least one precondition bit that is checked in the processor. Further, Claim 3 recites that the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled. Claim 3 has further been amended to recite that, if the post-condition is fulfilled, to check corresponding flag bits, and to drive a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction.

Summarily, Kadosumi and the Intel Guide, do not disclose, teach, or suggest each and every feature as recited by amended Claim 1. In particular, applicant submits that the Intel Guide does not qualify as prior art to the present application.

Once the examiner conducts a search and finds a printed publication which discloses the claimed invention, the examiner should determine the effective filing date of the application and compared with the date of the reference. (See MPEP 706.02) The examiner must determine the issue or publication date of the reference so that a proper comparison between the application and reference dates can be made. A magazine is effective as a printed publication under 35 U.S.C. 102(b) as of the date it reached the addressee and not the date it was placed in the mail. *Protein*

Foundation Inc. v. Brenner, 260 F. Supp. 519, 151 USPQ 561 (D.D.C. 1966). (See MPEP 706.02)

The present application claims is based on PCT Application No. PCT/EP00/09267 (hereinafter, "the '267 PCT Application"). Therefore, the present application is afforded the '267 PCT Application filing date of September 21, 2000 as the domestic priority date within the United States. Further, the present application claims priority to German Application DE 199 45 940.1 filed on September 24, 1999.

The Intel Guide has a date of copyright of 1999. Further, on its face, the Intel Guide has a date of May 1999. However, it is not clear if this May 1999 date is an actual date of publication where it was actually distributed to anyone in the public.

As stated above, the Intel Guide is an application developer's architecture guide for IA-64. The brand name of Intel's IA-64 processor is "Itanium". Attached as Exhibit A is a Wikipedia Web-Site page directed to the Itanium processor (http://en.wikipedia.org/wiki/Itanium). The Web-Site page states that the Itanium processor was developed between 1989 and 2001 and was introduced in June 2001. Thus, the Itanium processor was introduced to the public at a much later date than the date the present application can claim to domestic priority. Since the Itanium processor was made available to the public in 2001, it is very unlikely that the corresponding Developer's Architecture Guide, particularly the cited "IA-64 Application Developer's Architecture Guide" was actually made available to the public two years earlier. Therefore, the printed date on Intel's "IA-64 Application Developer's Architecture Guide", i.e. May 1999, is very likely not the date this document was

disclosed to the public, if at all. It is rather likely that Intel's "IA-64 Application Developer's Architecture Guide" was made to the public, if at all, around the time the Itanium processor was actually available, i.e. in 2001.

Further, even if the Intel Guide was distributed before the Itanium processor was made available to the public before 2001. No proof has been provided as to when the document was actually distributed. There is nothing to show that it was actually distributed before the domestic priority date of September 21, 2000 or even the foreign priority date of September 24, 1999. Company leaflets or product guides cannot be assumed to have automatically made their way to the public. Rather to the contrary it depends on the particular circumstances and the available evidence for that, to justify the assumption that such company papers were indeed available to the public at a particular date.

Thus, based on the evidence provided in Exhibit A and above and based on a lack of evidence as to the actual distribution date of the Intel Guide, applicant respectfully submits that it has not been proven that the Intel Guide qualifies as prior art to the present application.

For at least the reasons set forth above, the rejections of claims 1 and 3 based on Kadosumi and the Intel Guide should be withdrawn.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON, TAYLOR & HUNT, P.A.

Date: October 9, 2007

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